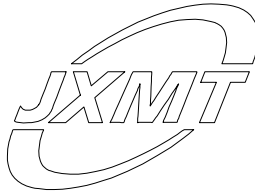
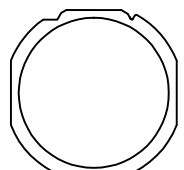
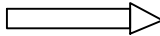
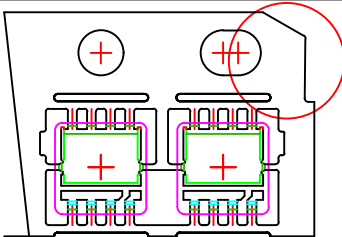
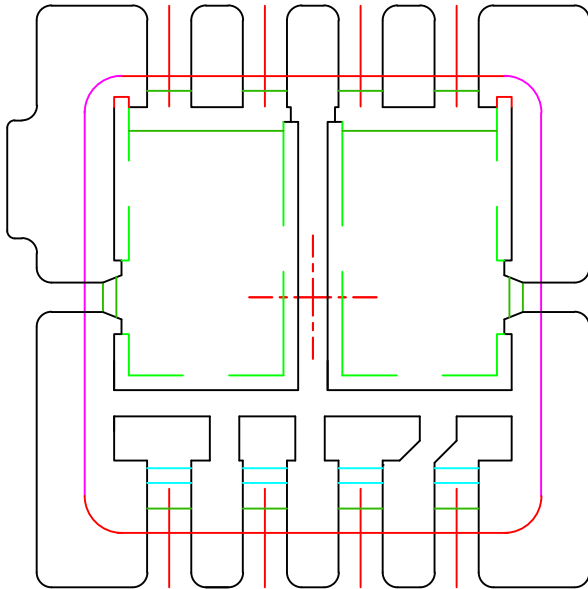


Bonding Diagram

	安徽积芯微电子科技有限公司 Anhui Jixin Microelectronics Technology Ltd.			
	BD No.		版本	
	Device		Package	PDFN3.3X3.3D
装片方向 	引线框传输方向 			客户确认



BOM	TYPE					
	Die Name	Wafer Size (inch)	Die Size Without SL(μm)	Gate Pad Size (μm)	Scribe Line (μm)	Die Thickness (μm)
芯片CHIP						
引线框物料号 L/F Material No:		栅极线材规格 Gate Wire Spec.		银胶 Epoxy		晶圆背金 Wafer back material
基岛尺寸 (mm) L/F Pad Size	1.2 * 1.76 * 2	源极线材规格 Source Wire Spec.		锡膏 Solder paste		晶圆正面金属 Wafer top material
电镀方式 L/F Plating Type		总线数 Total Qt'y		塑封料 Compound		
焊线方式 Wire Type		产品等级 MSL Level		电镀方式 Plating Type		
线图来源 BD source			备注 Remark			
制图日期			有效期	<input checked="" type="checkbox"/> 永久 <input type="checkbox"/> 六个月 <input type="checkbox"/> 其他		
拟制 Prepared By		审核 Checked By		批准 Approved By		文控发行章 Controlled Chapter